MicroConverter® Multi-Channel 12 Bit ADCs and DACs with Embedded Flash MCU

Silicon Anomaly Sheet — ADuC841/ADuC842/ADuC843

This anomaly list represents the known bugs, anomalies, and workarounds for the ADuC841/ADuC842/ADuC843 MicroConverter products. The anomalies listed apply to all ADuC841/ADuC842/ADuC843 packaged material is branded as follows:

Third Line F21

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended workarounds outlined here.

ADUC841/ADUC842/ADUC843 SILICON ANOMALY SHEET REVISION HISTORY

Revision	Date	Relevance	Silicon Status	Number of Bugs Reported
F.1	April 2005	All silicon branded Third Line: F21	Release	5

ANOMALIES

1. SPI INTERFACE [er006]

Background:	The SPI can either be used on the standard pins or can be moved to P3.3, P3.4 and P3.5 by setting the MSPI bit in CFG841/CFG842. When the MSPI bit is set P3.3 should be MISO, P3.4 MOSI and P3.5 SCLOCK.
Issue A:	By setting the MSPI bit the P3.3, P3.4 and P3.5 have the following configuration. P3.3 = MISO, P3.4 = SCLOCK, P3.5 = MOSI
Workaround A:	None.
Issue B:	When the ADuC841/ADuC842/ADuC843 is set up as an SPI slave the device may receive or transmit bytes incorrectly.
Workaround B:	None
Related Issues:	None

2. Reading/Writing To DATAFLASH/EE [er007]

Background:	There are 4kB of DATAFLASH/EE which can be used for non-volatile storage.
Issue:	If an interrupt occurs during a DATAFLASH/EE read or write operation, code execution may resume at a random program memory address.
Workaround:	Disable all interrupts prior to a read or write operation. This can be done by setting the EA bit to 0.
Related Issues:	None.

3. PWM Operation [er008]

Background:	The PWM output rate is determined by the PWMxH and PWMxL registers for the PWM0 and PWM1 outputs.
Issue:	Modifying RAM address 2EH causes the PWM timer to be reset.

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Workaround:	For Assembly code:	Do not use memory location 2EH.
	For C code:	Assign a dummy variable to location 2EH using the following code.....
		idata unsigned int ui32Dummy[2] _at_ 0x2E;
Related Issues:	None.	

4. Watchdog Timer [er009]

Background:	The ADuC841, ADuC842, and ADuC843 incorporate a Watchdog Timer. The purpose of the WDT is to ensure the part is never stuck in an endless loop by generating either a hardware reset or an interrupt event that vectors to the WDT ISR.
Issue:	If the WDT generates an interrupt as opposed to a hardware reset, and if the ISR subsequently access the WDT SFRs a minimum of 2 WDT clocks must be given to allow these instruction to execute correctly. The ISR must not be exited until this time has elapsed.
Workaround:	Add a delay of 2 x 1/32768 after any access to the WDT SFRs while in the ISR.
Related Issues:	None.

5. Level Triggered Interrupt Operation [er010]

Background:	The ADuC845/7/8 incorporate two external interrupt sources (INT0 & INT1) that can be configured to respond to either an edge event or a level event.
Issue:	If an interrupt occurs on the INT0 or INT1 pins and is then removed within one core instruction cycle, the interrupt vector address that is generated may be incorrect resulting in a vector to 0000H. This effectively restarts code execution.
Workaround:	To ensure that this does not occur the level triggered interrupt source must be kept low for a minimum of 9 core clock cycles.
Related Issues:	None.

6. SPI Operation [er011]

Background:	The SPI interface can be enabled as SLAVE or MASTER mode. In slave mode the master provides a clock signal on the SCLOCK pin.
Issue :	In SLAVE mode if external system noise on the SCLOCK pin causes a large number of clock inputs to be generated, the SPI interface can be put in a mode whereby it will no longer respond to SPI communication. In this mode all data sent to the SLAVE will be transmitted back by the slave on the subsequent SPI transfer.
Workaround :	Toggle the SPE bit in SPICON. This will reset the SPI interface and it will resume responding to SPI communications from a MASTER.
Related Issues:	None.

ADuC841/842/843 SILICON ANOMALY REVISION HISTORY

Anomaly No.	Description	Status
er001	MODE 0 UART OPERATION	Fixed
er002	USE OF THE EXTENDED STACK POINTER	Fixed
er003	USE OF I2C IN SLAVE MODE WITH STOP INTERRUPT ENABLED	Fixed
er004	USE OF I2C IN SLAVE MODE WITH STOP INTERRUPT DISABLED	Fixed
er005	I2C DATA TRANSFER	Fixed